REMARKS

Claims 1, 3-5, 7, 9, and 12-21 are presented for further examination. Claims 1, 3, 4, 7, 9, 13, 15, 16, 18, and 21 have been amended. Claims 2, 6, 8, 10, and 11 have been canceled.

In the Office Action mailed October 6, 2006, the Examiner rejected claims 1-21 under 35 U.S.C. § 103(a) as obvious over U.S. Patent Publication No. 2002/0194466 ("Catherwood") in view of U.S. Patent No. 6,401,154 ("Chiu").

Applicants respectfully disagree with the basis for the rejection of the claims and request reconsideration and further examination of the claims.

The disclosed and claimed embodiments of the invention are directed to a microcontroller device and method for managing program interrupts in the microcontroller device. These interrupts can occur during either normal operation, in which case they are managed by an arbiter (15), such as the instruction fetch 13 and the ALU 14, or to manage interrupts during iterative processing procedures managed by a dedicated processing module (12).

Catherwood, U.S. Patent Publication No. 2002/0194466, is directed to a processor for processing an interruptible repeat instruction. Catherwood does not describe or suggest the usage of an arbiter module, and therefore no separate interrupt management is utilized.

Although the usage of arbiters is generally known, the flexible interrupt management of the disclosed and claimed embodiments of the invention are in no way disclosed, suggested, or hinted at in the Catherwood reference. The Examiner has cited Chiu, U.S. Patent No. 6,401,154, as teaching the use of an arbiter in an interrupt controller. However, Chiu does not teach or suggest separate interrupt management through a processing module in combination with an arbiter module such that the processing module manages interrupts during iterative processing procedures.

Turning to the claims, claim 1 is directed to a microcontroller device that has a control unit with a plurality of logic modules that include a processing module for **iterative processing procedures**, an interrupt managing module for managing program interruptions caused by internal or external events, and an arbiter module for managing switching of the

plurality of modules. In other words, the arbiter module manages switching between the interrupt managing module that manages program interruptions caused by internal or external events and a separate processing module that executes iterative processing procedures. Claim 1 further recites a set of interruption registers associated with a control unit for storing information regarding interrupts and for requesting arrest of the processing module for iterative processing procedures, with the set of interruption registers including a register for served interrupts, a register containing information regarding which interrupt has interrupted execution of the processing module, and a register in which there is stored the state of the module for managing the processing procedure at which said interrupt has occurred.

As discussed above, nowhere do Catherwood and Chiu, taken alone or in any combination thereof, teach a control unit having logic modules that include a process module for iterative processing procedures, an interrupt managing module for managing program interruptions caused by internal or external events, and an arbiter module for managing switching of the plurality of modules along with the set of interruption registers as recited in claim 1. In view of the foregoing, applicants respectfully submit that claim 1 is clearly allowable.

Remaining dependent claims 3-5 are also allowable for the features recited therein as well as for the reasons why claim 1 is allowable.

Independent claim 7 is directed to a method for managing program interrupts in a microcontroller device that includes the processing module and interrupting managing module and includes the steps of upon occurrence of an interrupt in a state of the iterative processing procedure, transferring the control from the module for managing the iterative processing procedure to the interrupt managing module, storing in input registers information regarding the interrupt that has occurred by storing the served interrupt in a register of the served interrupts, storing the information regarding which interrupt has interrupted execution of the iterative processing procedure in a respective register, and storing the state of the module for managing the iterative processing procedure at which the interrupt has occurred in a further respective register. Claim 7 further recites at the end of the interrupt transferring control to the interrupt managing module for execution of an instruction of a return from interrupt type, and evaluating whether the interrupt has occurred on the iterative processing procedure rather than on the

processing procedure, and in the positive restoring the control to the module for managing the processing procedure at the state where the interruption occurred, and in the negative restoring the control to an arbiter module.

As discussed above, Catherwood does not disclose the usage of an arbiter module and the combination of Catherwood and Chiu does not disclose, teach, or suggest the flexible interrupt management as recited in claim 7 wherein upon occurrence of an interrupt in a state of an iterative processing procedure, transferring control to an interrupt managing module and then returning back to the state at which the interruption occurred in the iterative processing procedure module. In view of the foregoing, applicants respectfully submit that claim 7 is clearly allowable over the combination of Catherwood and Chiu. Dependent claims 9 and 12 are allowable for the features recited therein as well as for the reasons why claim 7 is allowable.

Claim 13 is directed to a microcontroller device that includes a processing module for iterative processing procedures and an interrupt managing module configured to manage program interruptions caused by internal and external events, and an arbiter module for managing switching of the processing module and the interrupt managing module within a control unit, and first, second, and third registers for storing interrupts, information regarding an interrupt, and the state of the processing module and managing the iterative processing procedure at the time the interrupt occurs, respectively, and a logic gate having a first input coupled to the first register and a second input coupled to the second register and an output coupled to the control module. Applicants respectfully submit that claim 13 is allowable over the combination of Catherwood and Chiu for the reasons discussed above with respect to claim 1, and that all claims depending from claim 13 are similarly allowable.

Independent claim 18 is directed to a method for managing program interrupts in a microcontroller device that includes, *inter alia*, receiving a control unit and interrupt in a state of an interruptive processing procedure, transferring control from the processing module to the interrupt managing procedure upon receipt of the interrupt, storing information regarding the interrupt into the set of interruption registers by the steps of storing recited in claim 1, processing the interrupt in a manner recited in claim 1, and transferring control of the interrupt managing module at the end of the interrupt to the processing module at the state at which the interrupt

occurred. Applicants respectfully submit that claim 18 and dependent claims 19 and 20 are allowable for the reasons discussed with respect to independent method claim 7.

Independent claim 21 is directed to a microcontroller device that includes the novel and non-obvious features discussed above with respect to claims 1 and 13. In view of the foregoing, applicants respectfully submit that claim 21 is also allowable over the combination of Catherwood and Chiu.

In view of the foregoing, applicants submit that all of the claims remaining in this application are now clearly in condition for allowance. In the event the Examiner disagrees or finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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